PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants:	Gschwind, et al.	**Examiner:**	Choi, Woo H.
Serial No.:	09/940,709	**Group:**	Art Unit 2189
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For:	**CONFIGURABLE MEMORY ARRAY**		

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REPLY BRIEF

In response to the Examiner's Answer dated January 25, 2008 Applicants submit this reply brief.

This reply brief is submitted to reflect the withdrawal of the rejection of Claims 22-37 under 35 USC 112, first paragraph and to rebut the rejection of Claim 29 under 35 USC 112, first paragraph. The reply brief reiterates the arguments presented in the appeal brief with respect to the remaining rejections.

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1. Real Party in Interest

The real party in interest is International Business Machines Corporation, the assignee of the entire right, title, and interest in and to the subject application by virtue of an assignment of record.

2. Related Appeals and Interferences

(None)

3. Status of Claims

Claims 1-37, are pending, stand rejected, and are under appeal.

A copy of the Claims as pending is presented in the Claims Appendix.

4. Status of Amendments

(None)

5. Summary of Claimed Subject Matter

For purposes of illustration, the invention of Claims 1, 22, 26, 29, 30 and 33, will be described with reference to the exemplary FIGS. and corresponding text of Appellants' Specification (hereinafter, Spec.), for example, but nothing herein shall be deemed as a limitation on the scope of the invention. In general, the claimed inventions are direct to systems and methods for implementing configurable memory systems in which memory can be configured for use suitable for a wide range of applications. For instance, FIG. 1 of Spec. illustrates an electronic device (100) having a reconfigurable memory (130) which can be selectively configured as a local main memory (FIG. 2) or as cache memory (e.g., L2 cache as in FIG. 3), for example, (see, generally e.g., Spec. p. 10, line 8 - p. 14, line 16).

Claim 1 recites:

> A memory system on a chip, comprising:
> a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, wherein the configurable memory comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array, in the first mode of operation.

An exemplary embodiment of Claim 1 may be described with reference to FIGS. 1 and 4 and relevant description in Spec. For example, FIGS. 1 and 4 generally depict a memory system (130) on a chip (100) having a configurable memory (130) having a first mode of operation wherein the configurable memory (130) is configured as a cache and a second mode of operation wherein the configurable memory (130) is configured as a local, non-cache memory (see, e.g., Spec. p. 14, line 18 ~ page 16, line 13). The configurable memory (130) comprises a memory array (410) (FIG. 4) The memory array (410) includes both tag bits and data bits are stored in a single data line in the memory array (410), in the first mode of operation (see, e.g.,

Spec. p. 18, 10-14).

Claim 22 recites:

> A memory system on a chip, comprising:
> a configurable Random Access Memory (RAM) array having a first mode of operation wherein the configurable RAM array is configured as a local, non-cache memory and a second mode of operation wherein the configurable RAM array is configured as a cache,
> wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

An exemplary embodiment of claim 22 may be described with reference to FIGS. 1 and 4 and relevant description in Spec. For example, FIGS. 1 and 4 generally depict a memory system (130) on a chip (100) having a configurable RAM array (410) having a first mode of operation wherein the configurable RAM array (410) is configured as a local, non-cache memory and a second mode of operation wherein the configurable RAM array is configured as a cache (see, e.g., Spec. p. 14, line 18 ~ page 16, line 13; p. 5, lines 5-15). The first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register (see, e.g., Spec., p. 15, lines 8-14, FIG. 4, element (420); and FIG. 5 (steps 550, 550a); p. 23, lines 3-17) and generating a control signal based on said comparison to select the first or second mode of operation (see, e.g., the mode selection logic 435 (FIG. 4), blocks 540-550 (FIG. 5), and block 655 (FIG. 6), and Spec., p. 24, lines 5-10).

Claim 26 recites:

> A data storage system, comprising:
> at least one microprocessor; and
> a configurable memory, integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that

emulates a local, non-cache memory and a second mode of operation that emulates a cache,

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation, wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

An exemplary embodiment of claim 26 may be described with reference to FIGS. 1 and 4 and relevant description in Spec. For example, FIGS. 1 and 4 illustrate a data storage system, comprising at least one microprocessor (100), and a configurable memory (130), integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that emulates a local, non-cache memory and a second mode of operation that emulates a cache, wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation, wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register(see, e.g., Spec., p. 15, lines 8-14, FIG. 4, element (420); FIG. 5 (steps 550, 550a); p. 23, lines 3-17) and generating a control signal based on said comparison to select the first or second mode of operation (see, e.g., the mode selection logic 435 (FIG. 4), blocks 540-550 (FIG. 5), and block 655 (FIG. 6), and Spec., p. 24, lines 5-10).

Claim 29 recites:

A memory system on a chip, comprising:

a processor; and

a configurable memory having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local

memory and the cache, wherein any of the three modes of operation may be selected at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

An exemplary embodiment of claim 29 may be described with reference to FIGS. 1 and 4 and relevant description in Spec. For example, FIGS. 1 and 4 illustrate a memory system on a chip (100), comprising a processor (120); and a configurable memory (130) having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local memory and the cache, wherein any of the three modes of operation may be selected at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register(see, e.g., Spec., p. 15, lines 8-14, FIG. 4, element (420); FIG. 5 (steps 550, 550a); p. 23, lines 3-17) and generating a control signal based on said comparison to select the first or second mode of operation (see, e.g., the mode selection logic 435 (FIG. 4), blocks 540-550 (FIG. 5), and block 655 (FIG. 6), and Spec., p. 24, lines 5-10).

Claim 30 recites:

A method for accessing data, comprising the steps of:
providing a configurable memory on a chip;
providing control logic on the chip for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;
configuring the configurable memory as a local, non-cache memory in the first mode of operation;
configuring the configurable memory as a cache in the second mode of operation; and
accessing the data from the configurable memory, based upon a mode of the configurable memory,
wherein the first mode of operation or the second mode of operation can

be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

An exemplary embodiment of the method of Claim 30 is illustrated in FIG. 6 and the corresponding description in Spec. In particular, FIG. 6 illustrates a method for accessing data, comprising the steps of providing a configurable memory on a chip (step 605), providing control logic on the chip for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation (step 610), configuring the configurable memory as a local, non-cache memory in the first mode of operation (step 680), configuring the configurable memory as a cache in the second mode of operation (step 685); and accessing the data from the configurable memory, based upon a mode of the configurable memory (step 690). (See, e.g., Spec., p. 24, line 14 ~ p. 26, line 2). The first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register (see, e.g., Spec. p. 23, lines 3-17) and generating a control signal based on said comparison to select the first or second mode of operation (see, e.g., the mode selection logic 435 (FIG. 4), blocks 540-550 (FIG. 5), and block 655 (FIG. 6), and Spec., p. 24, lines 5-10).

Claim 33 recites:

A method for accessing data, comprising the steps of:
providing a configurable memory in a package;
providing control logic in the package for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;
configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation, and

accessing the data from the configurable memory, based upon a mode of the configurable memory,

wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

An exemplary embodiment of the method of Claim 33 is illustrated in FIG. 6 and the corresponding description in Spec. In particular, FIG. 6 illustrates a method for accessing data, comprising the steps of providing a configurable memory in a package (step 650), providing control logic in the package for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation (step 655), configuring the configurable memory as a local, non-cache memory in the first mode of operation (step 680), configuring the configurable memory as a cache in the second mode of operation (step 685) and accessing the data from the configurable memory, based upon a mode of the configurable memory (step 690) (See, e.g., Spec., p. 24, line 14 ~ p. 26, line 2). The first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register (see, e.g., Spec. p. 23, lines 3-17) and generating a control signal based on said comparison to select the first or second mode of operation (see, e.g., the mode selection logic 435 (FIG. 4), blocks 540-550 (FIG. 5), and block 655 (FIG. 6), and Spec., p. 24, lines 5-10).

6. Grounds of Rejection to be Reviewed on Appeal

A. Claim 29 stands rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

B. Claims 1-8, 10-20 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,678,790 to Kumar.

C. Claims 1 and 21 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2002/0087821 to Saulsbury.

D. Claims 1, 10-14 and 21 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,321,318 to Baltz.

E. Claims 1-3, 6-10, 13-17, 20-23, 25, 26, 29, 30, 32 and 33 stand rejected as being anticipated under 35 U.S.C. §102(e) over U.S. Patent No. 6,868,472 to Miyake.

F. Claim 24 stands rejected as being unpatentable under 35 U.S.C. §103(a) over Miyake in view of U.S. Patent 6,377,912 to Sample, or in the alternative in view of U.S. Patent 6,611,796 to Natarajan.

G. Claims 27, 28, 31 and 34-37 stand rejected as being unpatentable under 35 U.S.C. §103(a) over Miyake in view of U.S. Patent 6,426,549 to Isaak.

7. Argument

A. The Claims Are Supported Under 35 U.S.C. §112, First Paragraph

i. Claim 29

Claim 29 has been rejected as failing to comply with the written description requirement. The Examiner contends that the specification does not support the claimed configurable memory with three modes of operation where any one of the modes is selectable at any time based on comparing an address to an address range contained in a configuration register.

Claim 29 claims, *inter alia*,

> a configurable memory having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local memory and the cache.

In assessing whether a specification satisfies the "written description" requirement under 35 U.S.C. 112, first paragraph, with respect to the claimed invention(s), the fundamental factual inquiry is whether the patent specification describes the claimed invention with *reasonable* clarity such that one of ordinary skill in the art can reasonably conclude that the inventor(s) had possession of the claimed invention as of the filing date of the specification. See *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed Cir. 1991). Compliance with the written description requirement does not compel use of any particular form of description, so long as the description clearly allows one of ordinary skill in the art to recognize that the applicant invented what is defined by the patent claims. See *In Re Alton*, 76 F.3d 1168, 1172 (Fed. Cir. 1996). Indeed, it is well established that the subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement.

See *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323 (Fed. Cir. 2000). "If a person of ordinary skill in the art would have understood the inventor to have been in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate description is met." *In re Alton*, 76 F.3d at 1175 (see also *Vas-Cath*, 935 F.2d at 1563).

The rejection does not present a prima facie case regarding the written description rejection of Claim 29. There is clear support for the claimed subject matter of Claim 29. For instance, the specification provides, at page 15, lines 3 ~ p. 16, line 13:

> The memory configuration logic 420 is further responsible for selecting the operating mode of the configurable memory array 130. Such selection of the operating mode may be based on, for example, the memory address, mode information received in conjunction with the memory address, a configuration register, a configuration signal, and/or other control information. That is, given the teachings of the present invention provided herein, one of ordinary skill in the related art will contemplate these and various other criteria upon which selection of the operating mode of the configurable memory array 130 can be based, while maintaining the spirit and scope of the present invention.
>
> The memory configuration logic 420 includes an array address mapping module 425, a control module 430, mode selection logic 435, tag match logic 440, and multiplexers 445 and 450. The configuration of the memory array 410 is controlled by the mode selection logic 435, which generates all necessary control and configuration signals. The mode of operation can be selected by . . . a function the memory address itself. These control logic components enable, for example, four modes of operation: local memory read mode; local memory write mode; cache read mode; and cache write mode. (emphasis added)

The above teachings provide clear and explicit support for the subject matter of claim 29.

Furthermore, the subject matter of Claim 29 is supported by the following teachings in Applicants' specification, at page 23, lines 3 ~ 17, and FIG. 5:

> Yet another exemplary configuration option is as follows. When the CPU 110 performs a memory access, the access mode of the configurable memory array 130 is selected based upon the address of the memory access (step 550). For example, when the CPU 110 performs a memory access, the supplied address

> of the access determines whether the memory array is to be treated as local memory or cache. This can be used to effectively partition the configurable memory array 130 into (1) a small high-speed local working memory for data processing and (2) a cache for access to a large system memory. The control information may be obtained by comparing the address to one or more address ranges contained in configuration register(s) (step 550a), or by performing any of a variety of logical operations on the address bits (step 550b).

The rejection seemingly relies on the above teachings to find that the "specification discloses only two modes of access for any given address - cache mode access and local memory mode access." This finding is unreasonable in view of the fact that there is no limiting language in the cited passage to support a finding that the invention is limited to selection of only two different modes based on the address of the memory acess. Indeed, the cited passage cites the two different modes by way of example. In any event, the specification is replete with specific support for Claim 29 (such as cited above) which clearly undermines such a restrictive finding.

Further still, the limitations of Claim 29 are supported at page 6, lines 3-11.

Irrespective of whether or not the subject matter of Claim 29 is explicitely described *in haec verba* in the specification, in order to support this 112 rejection, it is incumbant on the Examiner to explain why one of ordinary skill in the art would not reasonably conclude that the inventor(s) had possession of the claimed invention (of Claim 29) as of the filing date of the specification given the broad, non-limiting teachings in Applicants specification (as cited above) of using memory addresses for selecting multiple modes, with 2 and 4 modes as specifically described examples. Without such a showing, the 112 rejection should be withdrawn.

In response to the Examiner's Answer, and in particular the statement that "it is unclear how a single address can operate in both cache and local memory modes at the same time as claimed"; respectfully, the claim language is directed to a configurable memory having three modes of operation, and not a single address. Further, page 22, line 21 to page 23, lines 2 teaches

how to partition a configurable memory having a third mode of operation for emulating both the local memory and the cache. Accordingly, the configurable memory may be implemented as both a local memory and a cache type memory. Applicant respectuflly requests withdrawal of the rejection.

B. The Claim Rejections Under 35 U.S.C. §102 Are Legally Deficient

For a claim to be anticipated under 35 U.S.C. § 102, all elements of the claim must be found in a single prior art reference (see, e.g., *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d. 1001, 1010 (Fed. Cir. 1991)). The identical invention must be shown in as complete detail as is contained in the claim. (See MPEP § 2131). The single prior art reference must disclose all of the elements of the claimed invention functioning essentially in the same manner (see, e.g., *Shanklin Corp. v. Springfield Photo Mount Corp*, 521 F.2d 609 (1st Cir. 1975)).

Here, Applicants respectfully assert that the separate teachings of Kumar, Saulsbury, Baltz and Miyake are legally deficient to establish prima facie case of anticipation against the respective rejected claims for at least the following reasons.

i. Kumar Does Not Anticipate Claim 1

With regard to Claim 1, Applicants respectfully assert that Kumar does not disclose, for example, a configurable memory having *a memory array in which **both** tag bits and data bits are stored in a single data line in the memory array in a first mode of operation where the configurable memory is configured as a cache*, as claimed in Claim 1.

The rejection of Claim 1 is based, in part, on the Examiner's finding that Kumar discloses

a configurable memory having *"a memory array (12) in which both tag bits (figure 2, 50) and data bits (52) are stored in a single data line (col. 3, lines 32-33) in the memory array (figure 2, 12), in the second mode of operation.*" (See, p. 3 of the Final Action). As can be readily gleaned from the Examiner's Response to Arguments on p. 9 of the Final Action dated November 2, 2005, this finding is premised on the Examiner's finding that Kumar teaches *"forming a single logical data line in the memory array (12)"* based on Kumar's disclosure in Col. 3, lines 32-33 that each row of the tag array (50) corresponds to one of the data lines in the data array (52). From this, it appears that the Examiner determines that *"forming a single logical data line in the memory array (12)"* teaches a configurable memory array (12) that contains tag bits and data bits in the same array (12). This argument is not directly on point and is seemingly irrelevant to the specific claim language. Indeed, even assuming that the Examiner's characterization of Kumar as teaching a "single logical data line" is correct, the Examiner offers no explanation as to how the "single logical data line" is the same or similar to or otherwise anticipates the claim feature of *a memory array in which both tag bits and data bits are stored in a single data line in the memory array*, as in claim 1. Moreover, the Examiner's characterization of element (12) as being a memory array is seemingly incorrect as Kumar teaches a configurable memory system (12) having a plurality of separate memory arrays (50) and (52), for example. It should be noted that Claim 1 recites a configurable memory that comprises a memory array, and it is the memory array that stores both the tag and data bits in a single data line when the memory is in cache mode.

Furthermore, the Examiner's finding squarely contradicts Kumar's clear teaching of a reconfigurable memory (12) having separate memory arrays – a tag array (50) and a cache data array (52), for cache operation (as depicted in FIG. 2). Indeed, Kumar clearly discloses that the

data array (52) stores a data line and the tag array (50) stores sets of tags (Col. 3, lines 27-35). In other words, Kumar teaches that tag bits are not stored with data bits in a data line of a memory array configured as a cache (as in claim 1), but rather that data bits and tag bits are stored and accessed from different arrays. It should be noted that Applicants' Specification indicates that there is a difference between cache tags being stored in data lines stored in a memory array or having separate memory arrays for storing data and tags (see, Spec. page 18, lines 10-14). Accordingly, in view of the above, the Examiner has not sufficiently demonstrated how Kumar discloses, for example, a configurable memory having *a memory array in which **both** tag bits and data bits are stored in a single data line in the memory array in a first mode of operation where the configurable memory is configured as a cache*, as claimed in claim 1. Therefore, at the very least, the Final Action fails to present a *prima facie* case of anticipation of Claim 1 in view of Kumar. Further, Claims 2-8 and 10-20 are patentable over Kumar at least by virtue of their dependence from Claim 1.

Accordingly, withdrawal of the rejection is respectfully requested.

ii. Kumar Does Not Anticipate Claims 10-14

Claim 10 claims,

> the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses.

Claims 10-14 have been rejected seemly on the interpretation of the term "capable," wherein the Examiner stated essentially that "the claim only require a capability but not actual mode setting based on the addresses, this only requires that the structure can switch modes and can compare addresses, both of which are taught by Kumar."

Clearly, this argument fails to support a *prima facie* case of anticipation. The Examiner seems to place no patentable weight on the claim limitation of "*either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses*" on the ground that it is only a "capability" and not "required".

Assuming that the Examiner's characterization of the claims as reciting only a capability is correct, there is no legal or logical reason for Examiner's refusal to place patentable weight and consideration on a claim feature regarding a capability of a claimed device to perform a claimed function. Indeed, if a claimed device is capable of performing a claimed function, and that same claimed function is not supported or disclosed in the prior art, then the claim feature is a patentably distinguishing feature and should be considered.

It should be noted that the **MPEP Section 2173.05(g)** indicates that claim language such as "capable of" or "may be" serve to precisely define present structural attributes of interrelated component parts of the claimed assembly. In the case at bar, the claimed feature in which a first or second mode *can be* selected based on comparing a supplied address to at least one address range, is a definite, patentably distinguishing feature of Kumar. It should be further noted that Applicants Specification teaches that the claimed devices and methods may implement mode configuration options either individually or in combination (see, e.g., Spec. p. 20, lines 12-15). This provides clear support for claim language that a mode selection *can be* performed by a particular method, but not required to be performed by such method.

Moreover, there is no support for the Examiner's assertion that Kumar teaches a memory system that is capable of supporting a mode selection based on an address comparison. The Examiner fails to point to any specific teaching in Kumar to support such finding. The reason is simple - Kumar does not disclose or suggest any such mode selection feature (see, e.g., Kumar,

Col. 2, lines 47-60, where the disclosed mode selection options do not disclose or suggest the claimed mode selection features). Clearly, there is error in this analysis and the Examiner's failure to consider the claimed features constitutes reversible error.

Accordingly, withdrawal of the rejection is requested.

iii. Saulsbury Does Not Anticipate Claim 1

Applicants respectfully assert that Baltz is legally deficient to establish a *prima facie* case of anticipation against Claims 1 and 21. With regard to Claim 1, Applicants respectfully assert that Saulsburg does not disclose, for example, a configurable memory having *a memory array in which both tag bits and data bits are stored in a single data line in the memory array in a first mode of operation where the configurable memory is configured as a cache*, as claimed in Claim 1.

At the very least, the Examiner has not fairly demonstrated how Saulsbury teaches a configurable memory comprising *a memory array in which both tag bits and data bits are stored in a single data line in the memory array*, in the first mode of operation where the configurable memory operates as a cache, as recited in Claim 1. Saulsbury's general statement that a DRAM memory can be configured as "a cache memory with associated tags" does not teach or suggest the claimed limitation of *a memory array in which both tag bits and data bits are stored in a single data line in the memory array*. Saulsbury's teaching can more readily apply to associated tags that are stored in separate tag memories or libraries. In fact, FIG. 3 of Saulsbury discloses a separate caches (112) and (114) for data and tags (see also, paragraph [0037], first sentence). Thus, the teachings of Saulsbury do not support the anticipation rejection. Further, Claim 21 is patentable over Saulsbury at least by virtue of its dependence from Claim 1.

For at least the foregoing reasons, withdrawal of the rejection is respectfully requested.

iv. Baltz Does Not Anticipate Claim 1

Applicants respectfully assert that Baltz is legally deficient to establish a *prima facie* case of anticipation against Claims 1, 10-14 and 21. At the very least, Baltz does not disclose a configurable memory that comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array in a first mode of operation where the configurable memory is configured as a cache, as claimed in Claim 1.

The basis for Examiner's rejection of claim 1 in view of Baltz is set forth on page 7 of the Final Action dated June 4, 2007. The Examiner contends that FIG. 9, elements 30, 31 and 32 illustrate a memory array for storing tag bits and data bits in a single data line in the memory array. However, similar to those arguments presented above with regard to Claim 1 in view of Kumar, Baltz teaches separate tag memories (33, 32) (FIG. 9) of a memory controller (30) that are distinct from the memory data array (31) (see for example, FIG. 1). Accordingly, for at least the above reasons, Claim 1 is patentably distinct from Baltz. Claims 10-14 and 21 are patentable over Baltz at least by virtue of their dependence from Claim 1.

Accordingly, withdrawal of the rejection is requested.

v. Baltz Does Not Anticipate Claims 10-14

It should be noted that Claims 10-14 are further patentable over Baltz for similar reasons discussed above with respect to Kumar. The Examiner's rejection of Claims 10-14 is not based on cited art, but rather because the claim language recites a capability (see Claim 10, which recites in part, "wherein the configurable memory is capable of…"). Thus for similar reasons

given above, the Examiner's rejection of Claims 10-14 constitutes reversible error.

Accordingly, withdrawal of the rejection is respectfully requested.

vi. Miyake Does Not Anticipate Claims 1-3, 6-10, 13-17, 20-23, 25, 26, 29, 30, 32 and 33

Applicants respectfully assert that Miyake is legally deficient to establish a *prima facie* case of anticipation against Claims 1-3, 6-10, 13-17, 20-23, 25, 26, 29, 30, 32 and 33. With regard to Claims 1, 22, 26, 29, 30 and 33, Applicants respectfully assert that Miyake does not disclose, for example, *a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory*, as claimed in Claim 1 and essentially as claimed in Claim 30, nor *generating a control signal based on said comparison to select the first or second mode of operation*, as claimed in Claims 22, 26, 29, 30 and 33.

In formulating the rejections based on Miyake, the Examiner relies on various embodiments by mixing different elements to establish anticipation. However, anticipation is not properly established in that manner. For instance, the Examiner cites the embodiment in FIG. 35 of Miyake (Col 34, lines 40-50) to show a cache portion (320) having a storage part (326) that functions as a cache memory or a random access memory. However, FIG. 37 illustrates that the tags (307) are separate from the storage part (326) when the system of FIG. 35 operates in cache mode. The Examiner instead relies on a different embodiment of FIG. 8 to shown tag and data stored in a cache lines. However, FIG. 8 illustrates a direct-mapped unified cache architecture (see, Col. 9, lines 43-44), which does not operate in different cache or RAM modes. These elements have been selected from distinct, and not combinable, embodiments of the Miyake reference to establish anticipation. For at least these reasons, no prima facie case of

anticipation has been established for Claims 1 and 30 based on Miyake.

Moreover, the claims have been amended to clarify essentially that one of multiple modes of are selectable during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select one of the modes of operation, essentially as claimed in Claims 22, 26, 29, 30 and 33.

In Col. 37, lines 7-47, Miyake teaches that a CPU sends control signals to set flags in the cache controller (325) so that cache ways can be configured as RAMs and to cause RAM address registers (various units (321~324)) to hold required address values that correspond to the address spaces of the cache memory 326 acting as RAMs. In this regard, Miyake does not specifically disclose *comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select one of the modes of operation,* as generally recited in Claims 22, 26, 29, 30, and 33.

Claims 2, 3, 6-10, 13-17, 20, 21, 23, 25 and 32 are patentable over Miyake at least by virtue of their dependence from the respective independent claims.

Accordingly, withdrawal of the rejection is requested.

C. The Claim Rejections Under 35 U.S.C. §103 Are Legally Deficient

In rejecting claims under 35 U.S.C. §103, the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. *In re Rijckaert*, 9 F.3d 1531, 1532 (Fed. Cir. 1993). The burden of presenting a *prima facie* case of obviousness is only satisfied by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. *In*

re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988). A *prima facie* case of obviousness is established when the teachings of the prior art itself would appear to have suggested the claimed subject matter to one of ordinary skill in the art. In re Bell, 991 F.2d 781, 782 (Fed. Cir. 1993). If the Examiner fails to establish a *prima facie* case, the rejection is improper and must be overturned. In re Rijckaert, 9 F.3d at 1532 (citing In re Fine, 837 F.2d at 1074).

i. The Combined Teachings of Mikaye and Sample, or in the Alternative Mikaye and Natarajan Do Not Anticipate Claim 24

Claims 24 is patentable over the combined teachings of Mikaye and Sample or in the alternative, Mikaye and Natarajan at least by virtue of its dependence from Claim 22.

Accordingly, withdrawal of the rejection is requested.

ii. **The Combined Teachings of Mikaye and Isaak Do Not Anticipate Claims 27, 28, 31 and 34-37**

Claims 27, 28, 31 and 34-37 are patentable over the combined teachings of Miyake and Isaak at least by virtue of their dependence from the respective independent claims.

Accordingly, withdrawal of the rejection is requested.

D. Conclusion

Claim 29 has been shown to be supported by the specification. Further, the claimed invention is not disclosed or suggested by the teachings of the applied prior art references, either alone or in combination. Moreover, the Examiner has failed to establish a case of anticipated of the presently claimed method under 35 U.S.C. §102 in view of Kumar, Saulsbury, Baltz, or Miyake with respect to the respective independent claims. Accordingly, it is respectfully requested that the Board overrule the rejections of Claims 1-37.

Respectfully Submitted,

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8. CLAIMS APPENDIX

1. A memory system on a chip, comprising:

a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, wherein the configurable memory comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array, in the first mode of operation.

2. The memory system of claim 1, wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by an other selection of an other of the first mode of operation and the second mode of operation.

3. The memory system of claim 1, wherein the first mode of operation or the second mode of operation is selected at the burn-in time.

4. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a power-up time.

5. The memory system of claim 4, wherein the first mode of operation or the second mode of operation is selected at the power-up time using an external signal

6. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected during a program

execution.

7. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is selected during the program execution based upon a value of a special configuration register.

8. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is selected during the program execution based upon a value of an external signal.

9. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is selected during the program execution based upon comparing a supplied address to at least one address range contained in at least one configuration register.

10. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses.

11. The memory system of claim 10, wherein the range of addresses are determined at a burn-in time.

12. The memory system of claim 10, wherein the range of addresses are determined at a boot-up time.

13. The memory system of claim 10, wherein the range of addresses are determined dynamically.

14. The memory system of claim 10, further comprising a configuration register for storing the range of addresses.

15. The memory system of claim 1, wherein the configurable memory comprises:

memory configuration logic for selecting the first mode of operation or the second mode of operation.

16. The memory system of claim 1, wherein the configurable memory is capable of selecting one of a local memory read mode and a local memory write mode in the first mode of operation and is further capable of selecting one of a cache read mode and a cache write mode in the second mode of operation.

17. The memory system of claim 2, wherein the selection may be overridden by the other selection dynamically.

18. The memory system of claim 1, wherein the configurable memory comprises a plurality of static random access memory cells.

19. The memory system of claim 1, wherein the configurable memory comprises a

plurality of dynamic random access memory cells.

20. The memory system of claim 1, wherein the configurable memory is capable of being dynamically employed as a sole memory serving the processor and as a portion of a larger, memory hierarchy.

21. The memory system of claim 1, wherein the first mode of operation and the second mode of operation are employed concurrently.

22. A memory system on a chip, comprising:

a configurable Random Access Memory (RAM) array having a first mode of operation wherein the configurable RAM array is configured as a local, non-cache memory and a second mode of operation wherein the configurable RAM array is configured as a cache,

wherein either the first mode of operation or the second mode of operation is selectable during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

23. The memory system of claim 22, further comprising control logic for selectively providing direct access to the configurable RAM array as the local, non-cache memory in the first mode of operation and as the cache in the second mode of operation.

24. The memory system of claim 22, wherein a single logical line spans several physical

macro cells.

25. The memory system of claim 22, further comprising:

tag match logic for determining a match between the stored tag bits and bits corresponding to a memory access; and

at least one multiplexer for selecting and outputting data corresponding to the memory access, when the match is determined.

26. A data storage system, comprising:

at least one microprocessor; and

a configurable memory, integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that emulates a local, non-cache memory and a second mode of operation that emulates a cache,

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation, wherein either the first mode of operation or the second mode of operation is selectable during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

27. The data system of claim 26, wherein the at least one microprocessor and the configurable memory array are integrated on a single chip.

28. The data system of claim 26, wherein the at least one microprocessor and the configurable memory array are integrated in a single package.

29. A memory system on a chip, comprising:

a processor; and

a configurable memory having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local memory and the cache,

wherein any one of the three modes of operation is selectable at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second or third mode of operation.

30. A method for accessing data, comprising the steps of:

providing a configurable memory on a chip;

providing control logic on the chip for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;

configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation, wherein the configurable memory comprises a memory portion for storing tag bits and data bits

in a single data line in the memory portion, in the second or third mode of operation; and

accessing the data from the configurable memory, based upon a mode of the configurable memory,

wherein the either first mode of operation or the second mode of operation is selectable during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

31. The method of claim 30, further comprising the steps of:

providing at least one microprocessor for servicing memory access instructions for the configurable memory; and

integrating the at least one microprocessor with the configurable memory on the chip.

32. The method of claim 30, wherein the chip comprises a single chip.

33. A method for accessing data, comprising the steps of:

providing a configurable memory in a package;

providing control logic in the package for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;

configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation,

wherein the configurable memory comprises a memory portion for storing tag bits and data bits in a single data line in the memory portion, in the second mode of operation; and

accessing the data from the configurable memory, based upon a mode of the configurable memory,

wherein either the first mode of operation or the second mode of operation is selectable during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select the first or second mode of operation.

34. The method of claim 33, further comprising the steps of:

providing at least one microprocessor for servicing memory access instructions for the configurable memory; and

integrating the at least one microprocessor with the configurable memory in the package.

35. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a chip stack technique.

36. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a flip chip technique.

37. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a multi-chip module.

9. EVIDENCE APPENDIX

(None)

10. RELATED PROCEEDINGS APPENDIX

(None)